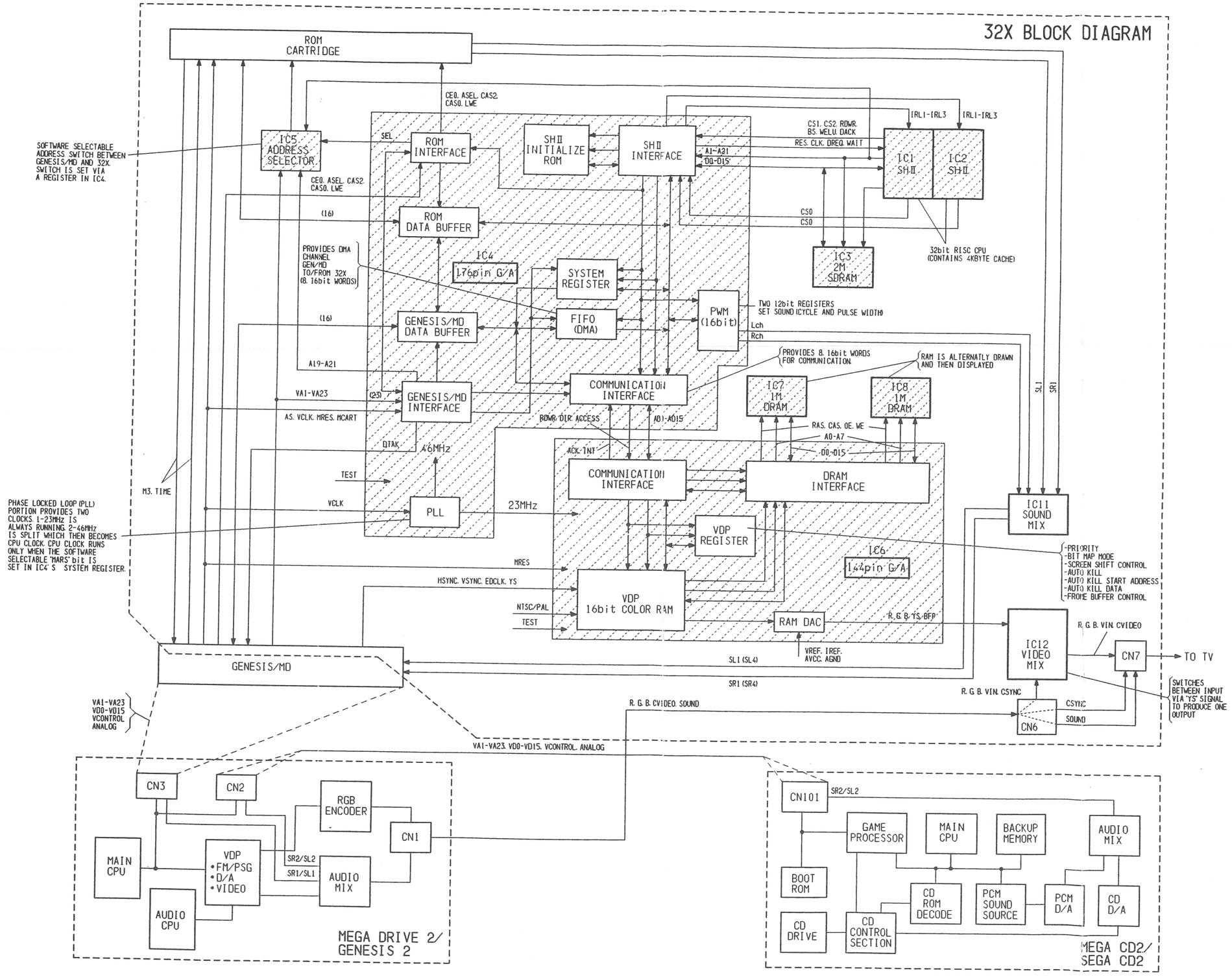
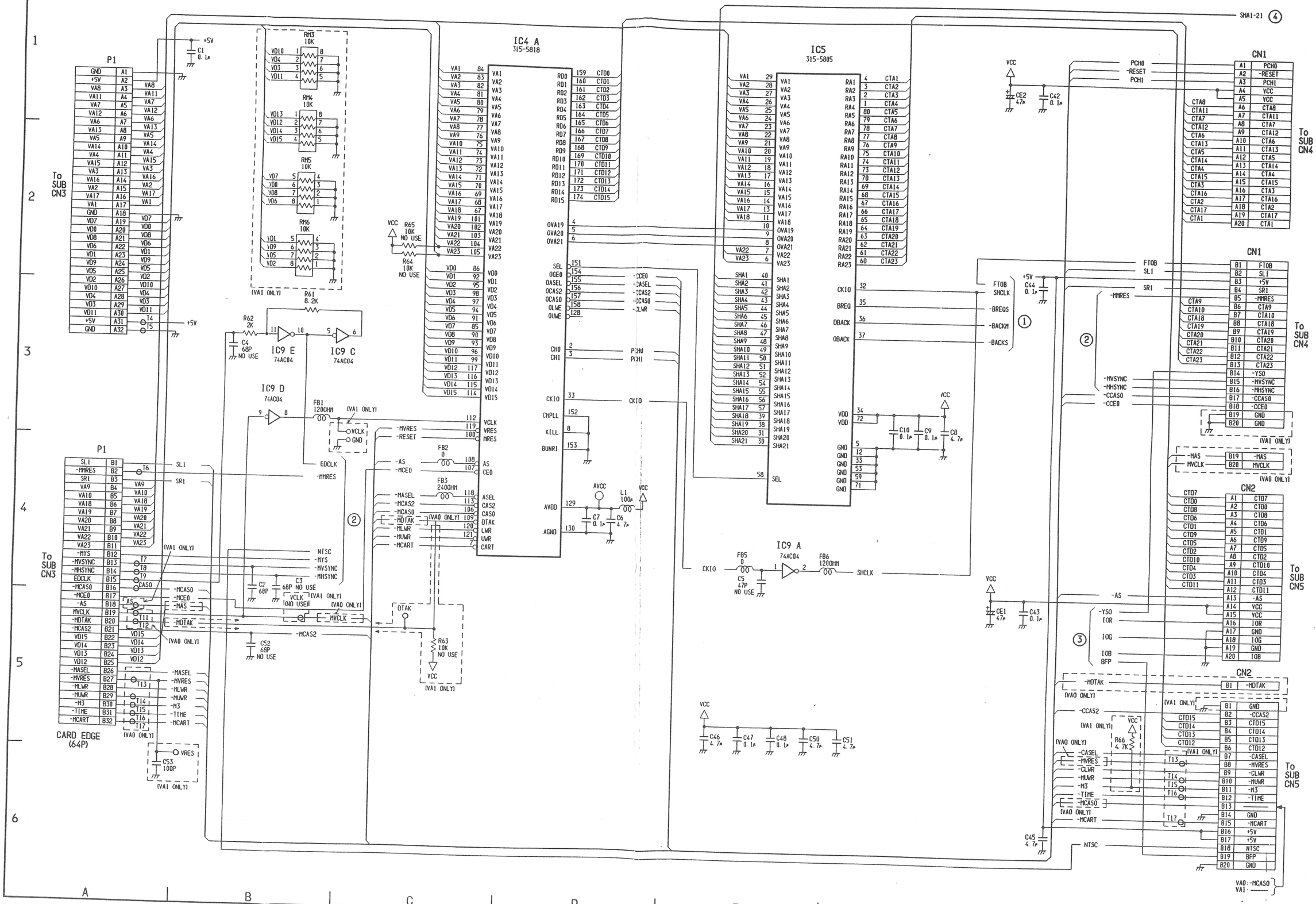
6. BLOCK DIAGRAM

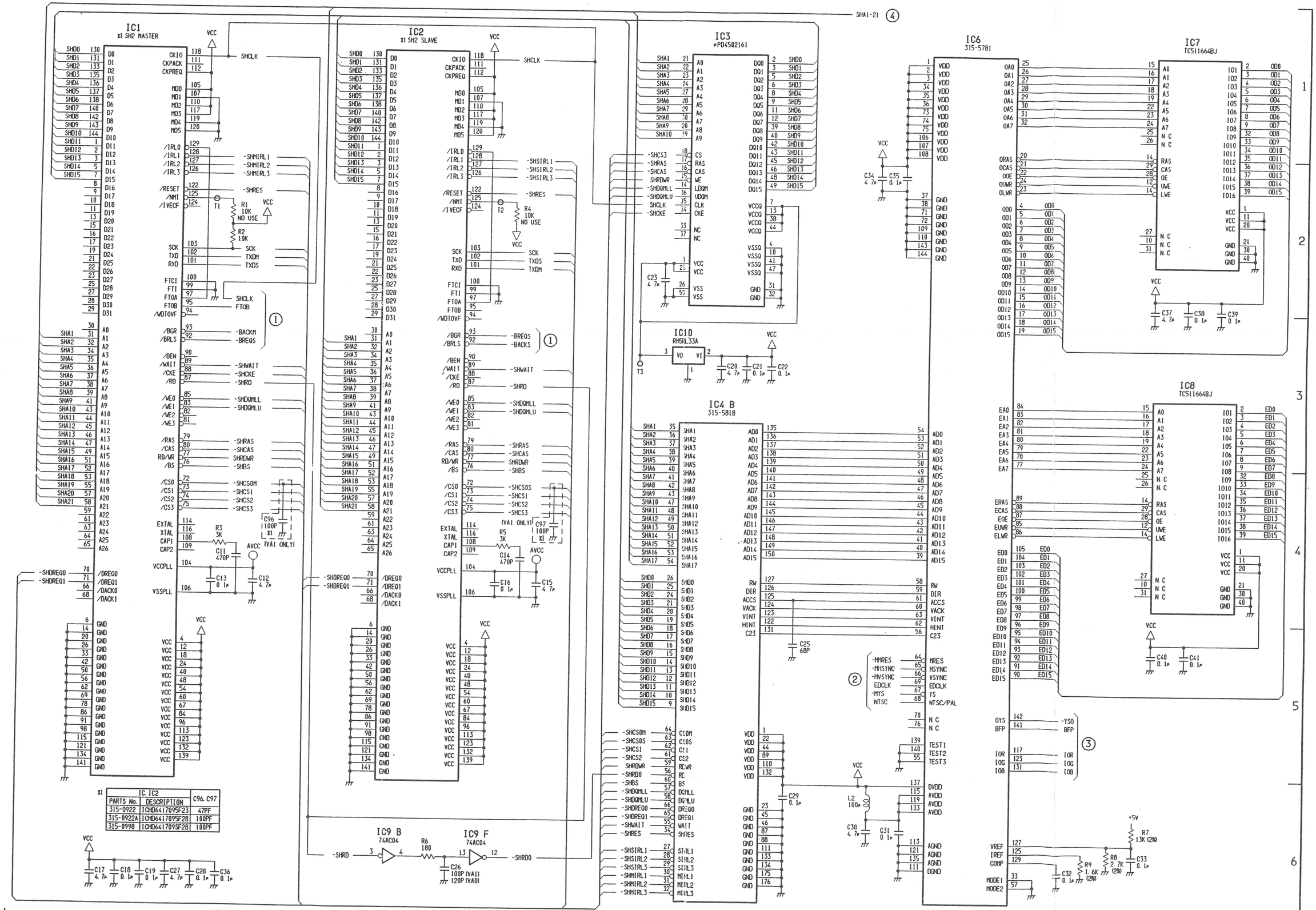


7. SCHEMATIC & CIRCUIT BOARD DIAGRAMS

7-1. Schematic Diagram-1(Main Section – 1/2)



7-3. Schematic Diagram-2 (Main Section – 2/2)



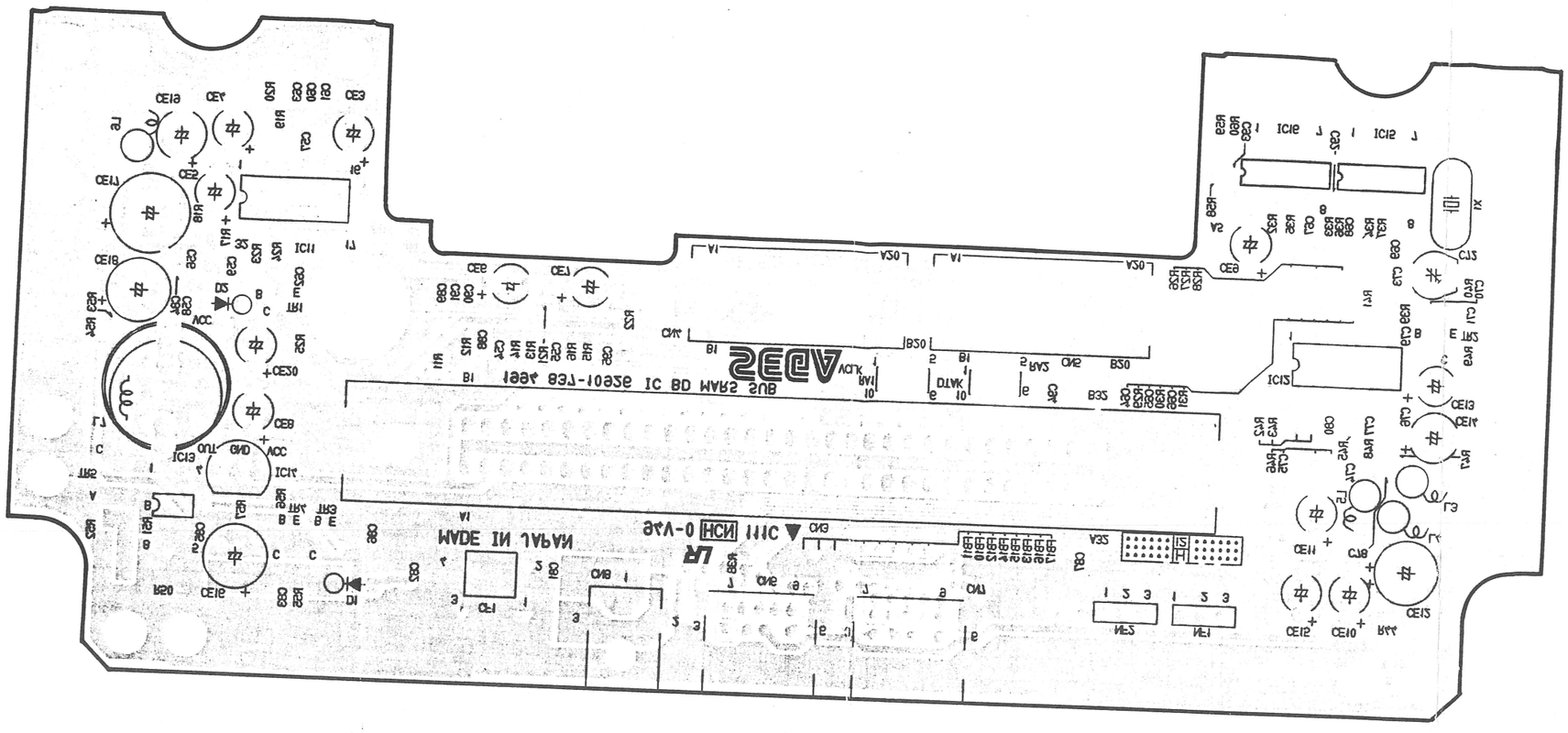
IC IC2		C96. C97
PARTS No.	DESCRIPTION	
315-0922	ICHD6417095F23	47PF
315-0922A	ICHD6417095F28	100PF
315-0998	ICHD6417095F28	100PF

7-4. Schematic Diagram-3 (Sub Section)

※ DIFFERENCE TABLE FOR DIAGRAM-3

※	CIRCUIT NO.	NTSC	PAL
1	L4	12㎌H	10㎌H
2	L5	100㎌H	82㎌H
3	X1	3.579545MHz	4.43361875MHz
4	R40	560	430
5	R41	1.2K	680
6	R42	1K	NOT USED
7	R43	NOT USED	1K
8	C70	47P	68P
9	C74	18P	15P
10	C75	56P	47P
11	C78	100P	82P

7-5. Circuit Board Diagram-2 (Sub Board)



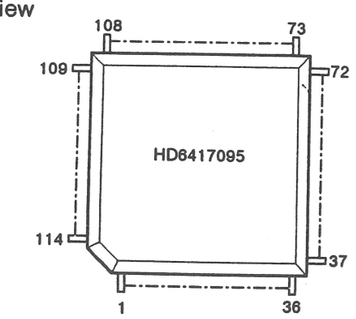
8. PARTS SPECIFICATIONS

IC1/2 CPU

IC HD6417095F23 QFP
Parts No. : 315-0922

IC HD6417095F28 QFP
Parts No. : 315-0922A

■ Top View



■ Description

No.	I/O	Pin Name	Function
1	I/O	D11	Data bus
2		D12	
3		D13	
4	–	VCC1	Power supply (5V)
5	I/O	D14	Data bus
6	–	VSS1	Power supply (0V)
7	I/O	D15	Data bus
8		D16	
9		D17	
10		D18	
11		D19	
12	–	VCC2	Power supply (5V)
13	I/O	D20	Data bus
14	–	VSS2	Power supply (0V)
15	I/O	D21	Data bus
16		D22	
17		D23	
18	–	VCC3	Power supply (5V)
19	I/O	D24	Data bus
20	–	VSS3	Power supply (0V)
21	I/O	D25	Data bus
22		D26	
23		D27	
24	–	VCC4	Power supply (5V)
25	I/O	D28	Data bus
26	–	VSS4	Power supply (0V)
27	I/O	D29	Data bus
28		D30	
29		D31	
30	I/O	A0	Address bus
31		A1	
32		A2	
33	–	VSS5	Power supply (0V)
34	I/O	A3	Address bus
35		A4	
36		A5	
37		A6	
38		A7	
39		A8	
40	–	VCC5	Power supply (5V)
41	I/O	A9	Address bus
42	–	VSS6	Power supply (5V)
43	I/O	A10	Address bus
44		A11	
45		A12	
46		A13	
47		A14	
48	–	VCC6	Power supply (5V)
49	I/O	A15	Address bus
50	–	VSS7	Power supply (0V)
51	I/O	A16	Address bus
52		A17	
53		A18	
54	–	VCC7	Power supply (5V)
55	I/O	A19	Address bus
56	–	VSS8	Power supply (0V)
57	I/O	A20	Address bus
58		A21	
59		A22	
60	–	VCC8	Power supply (5V)
61	I/O	A23	Address bus
62	–	VSS9	Power supply (0V)
63	I/O	A24	Address bus
64		A25	
65		A26	
66	O	DACK0	DMAC0 acknowledge
67	–	VCC9	Power supply (5V)
68	O	DACK1	DMAC1 acknowledge
69	–	VSS10	Power supply (0V)
70	I	DREQ0	DMAC0 request
71	I	DREQ1	DMAC1 request
72	O	$\overline{CS0}$	Chip select 0
73	O	$\overline{CS1}$	Chip select 1
74	O	$\overline{CS2}$	Chip select 2
75	O	$\overline{CS3}$	Chip select 3
76	I/O	$\overline{BS}$	Bus cycle start
77	I/O	RD/$\overline{WR}$	Read write
78	–	VSS11	Power supply (0V)
79	O	$\overline{RAS}$, $\overline{CE}$	RAS for DRAM/SDRAM/CE for PSRAM
80	O	$\overline{CAS}$, $\overline{OE}$	CAS for SDRAM/OE for PSRAM
81	O	$\overline{CASHH}$, DQMUU, $\overline{WE3}$	Each memory most significant byte select signal
82	O	$\overline{CASHL}$, DQMUL, $\overline{WE2}$	Each memory 2nd byte select signal
83	O	$\overline{CASLH}$, DWMLU, $\overline{WE1}$	Each memory 3rd byte select signal
84	–	VCC10	Power supply (5V)
85	O	$\overline{CASLL}$, DQMLL, $\overline{WE0}$	Each memory least significant byte select signal
86	–	VSS12	Power supply (0V)
87	O	$\overline{RD}$	Read pulse
88	O	CKE	SDRAM clock enable control
89	I	$\overline{WAIT}$	Hardware wait request.
90	O	$\overline{BEN}$	Reserve
91	–	VSS13	Power supply (0V)
92	I	$\overline{BACK}$, $\overline{BRLS}$	Bus right permission in slave mode./Bus right acknowledge in master mode.
93	O	$\overline{BREQ}$, $\overline{BGR}$	Bus right request in slave mode./Bus right acknowledge in master mode.
94	O	$\overline{WDTOVF}$	Watch dog timer qutput.
95	O	FTOB	Free-running timer output B.
96	–	VCC11	Power supply (5V)
97	O	FTOA	Free-running timer output A.
98	–	VSS14	Power supply (0V)
99	I	FTI	Free-running timer input.
100	I	FTCI	Free-running timer clock input.
101	I	RXD	Serial data input.
102	O	TXD	Serial data output.
103	I/O	SCK	Serial clock input/output.